A 56-GHz *LC*-Tank VCO With 17% Tuning Range in 65-nm Bulk CMOS for Wireless HDMI

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***Abstract*—A voltage-controlled oscillator (VCO) with a central frequency of 56 GHz and a 17% tuning range is presented. The oscillation frequency is tuned both by an analog input and by a 3-bit digital control bus using the same type of differential varactors. It achieves a record figure of merit, considering tuning range of 186.8 dBc/Hz and is able to address the full wireless high-definition multimedia interface band . The VCO is implemented in a 65-nm bulk CMOS process and dissipates 15 mW from a 1.2-V supply. Both fixed and parameterized electromagnetic models for inductors, interconnection structures, and transmission lines have been embedded in the classical design flow including layout verification and extraction, resulting in a very high level of simulation accuracy.**

***Index Terms*—CMOS voltage-controlled oscillators (VCOs), millimeter-wave integrated circuits, wireless high-definition multimedia interface (HDMI).**

I. Introduction

THIS PAPER presents a digital and voltage-controlled oscillator (VCO) that covers the 60-GHz millimeter-wave band including process, voltage, and temperature (PVT) variations for wireless high-definition multimedia interface (HDMI) applications. The spectrum allocation for this band has recently been disclosed by IEEE.802.15.3c Standard [1], as shown in Fig. 1. The available bandwidth is 7 GHz. The gigabit per second data rate required by wireless HDMI applications is achieved by combining wireless communication over a 60-GHz (indoor) and 1-Gbit Ethernet (GbE) local area network (LAN)/metropolitan area network (MAN) technology. Implementation is focused on the lowest possible cost per bit per second by developing highly integrated radio front ends based on silicon technologies. Implementation in silicon allows single-chip integration of the millimeter-wave front end, thus enabling a dramatic reduction in size and cost. For such application, low phase noise (PN) [or $\mathcal{L}(\Delta f)$], low-power, low-cost VCOs with a large frequency tuning range (FTR) are required. The tradeoff between power consumption, PN and FTR can be addressed using *LC*-tank VCOs implemented in CMOS technologies [2]–[13]. Ultra low power and low PN have been reported in previous works based in engineering the tank inductor using a slow-wave propagation mode, but at the expense of the FTR [2]. An FTR of 20% is obtained in [3] by using distributed VCOs at the expense of a large power consumption and area. The best compromise for FTR, PN, and power consumption can be obtained using *LC*-tank VCOs by optimally sizing the VCO transistors in order to minimize the parasitic capacitances and by maximizing the varactor capacitance range [4]–[13]. Our study demonstrates that very large tuning ranges (17%) can be achieved at millimeter-wave frequencies in bulk CMOS advanced processes, using an *LC*-tank VCO with differential accumulation-mode varactors and a combination of continuous tuning and digital switching of varactor banks, resulting in state-of-the-art PN and figure-of-merit (FOM) performances. Indeed, to the best of the authors' knowledge, it is the first *LC*-tank VCO that is able to address the full bandwidth of wireless HDMI including an extra frequency range for PVT compensation. The detailed structure and design process of the VCO is presented in Section II. The tank components are described in Section III, including a novel way of implementing transistorless switched capacitances for digital tuning of the VCO frequency. Section IV addresses the physical design and the techniques used to include the electromagnetic (EM) models of certain parts of the circuit along with the pcell models of the devices from the design kit seamlessly in the classical verification and post-layout simulation flow. Section V presents the experimental results and some comparisons with simulations, and finally Section VI concludes the paper by comparing the proposed VCO with the state of the art.

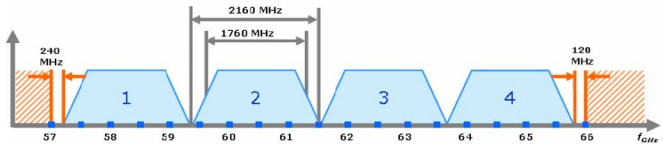

Fig. 1. IEEE.802.15.3c channel allocation.

II. Circuit Description and Design Process

A. Circuit Description

Fig. 2 shows the VCO schematic. The oscillator core is composed of an NMOS cross-coupled pair (MN1, MN2) and an *LC* tank. The tank inductance is a single-turn inductor with a central tap. It achieves a quality factor $Q_L = 18$ at 60 GHz.

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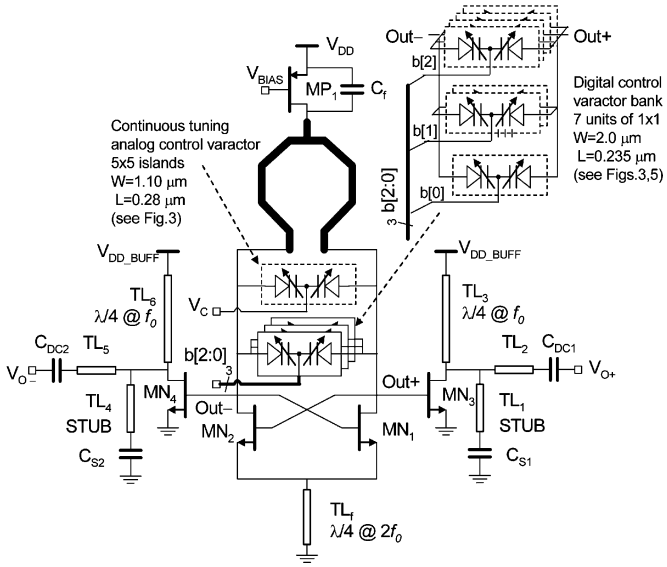


Fig. 2. VCO and output buffers schematic.

A differential N+poly/Nwell varactor operating in accumulation mode is used for continuous tuning. While previous works used two single-ended varactors connected in series [2]–[12], the differential varactor used in our VCO leads to an increased quality factor by reducing the differential current path length through the Nwell [14] and provides a smaller minimum capacitance due to the reduction of the routing interconnections. An additional bank of digitally controlled differential varactors provides coarse tuning for PVT calibration using three bits (b_2, b_1, and b_0). It is implemented with seven equal differential varactors grouped in 4, 2, and 1 units that change the binary-scaled capacitance. The binary switched varactors are made from the same structure as the fine-tuning varactor. A more detailed description of such varactors is provided in Section III.

The VCO core circuit is completed with a $2f_o$ filter composed of capacitor C_f and an inductor implemented with a microstrip transmission line (TL) (TL_f). This filter helps reduce the PN by lowering the contribution of flicker noise sources [15]. For test purposes, the output buffers are implemented by a common source stage $(MN_{3,4})$. They receive a separate power supply (V_{DD_BUFF}) through a $\lambda/4$ TL $(\mathrm{TL}_{3,6})$. The output is connected to the output pad through another microstrip $(\mathrm{TL}_{2,5})$ and a dc blocking capacitor $(C_{\mathrm{dc}1,2})$. The output impedance is matched to 50 Ω by adjusting the length of the output TL and the terminating capacitor value of an ac-short terminated stub $(T_{L1,4}$ and $C_{S1,2})$ that is connected at the drain of the buffer transistor.

B. Design Process

The VCO design process is summarized in this section. The next sections contain detailed descriptions of the tank components and the modeling approaches used throughout the process. It is important to note that only pcells from the technology design kit were used. The first step of the design process was to select the tank inductor. A large inductance value would facilitate the selection of the varactor, but leads to a lower quality factor and a small margin for parasitic capacitances. A small value requires a larger varactor capacitance range to cover the required frequency band but provides a large quality factor and self-resonant frequency. An inductor with $L = 95$ pH at dc was selected as a good tradeoff between these two ends. The available pcell model is a lumped equivalent circuit qualified up to 50 GHz. An EM analysis of the component was made in order to obtain a more accurate model that is valid at higher frequencies.

The wireless HDMI bandwidth is 7 GHz. An additional margin is required in the VCO in order to compensate for PVT variations. The 7-GHz tuning range is implemented using a varactor with continuous tuning, and the additional margin for PVT compensation is implemented using a digitally controlled bank of switched capacitors, as described in the following section. The continuous tuning range $f_{\max} - f_{\min}$, along with the center frequency $f_o = 0.5(f_{\max} + f_{\min})$, and the inductor set the value of the varactor [16]

$$\Delta C \geq 4\frac{(f_{\max} - f_{\min})}{L\pi^2(f_{\max} + f_{\min})^3}. \tag{1}$$

The selected varactors have a capacitance range ratio $C_{\mathrm{vmax}}/C_{\mathrm{vmin}} = 3$. Since $\Delta C = C_{\mathrm{vmax}} - C_{\mathrm{vmin}}$, the varactors are sized so that $C_{\mathrm{vmax}} = 2\Delta C/3$. An additional fixed capacitance (C_F) is required to set the lower bound of the frequency range

$$f_{\min} = \frac{1}{2\pi\sqrt{L(C_{\mathrm{vmax}} + C_F)}}. \tag{2}$$

The tank is simulated to obtain the parallel equivalent losses and the required transconductance of the cross-coupled NMOS pair that implements the negative resistance of the oscillator. This results in an NMOS transconductance $g_m = 20$ mS to guarantee oscillation startup. The size and bias current of the active section is determined by the dc output voltage of the VCO, which sets the common mode voltage for the differential varactors and the gate-to-source voltage (V_{GS}) for the NMOS transistors. A 780-mV voltage is selected since this value maximizes the capacitance excursion of the varactors and is very close to the V_{GS} that sets the peak g_m/W for the transistors. Minimum length transistors in this technology achieve the peak g_m/I_D for $V_{\mathrm{GS}} = 0.85$ V, as shown in Fig. 3. For $V_{\mathrm{GS}} = 0.78$ V and $g_m = 20$ mS, the minimum length NMOS transistors must have $W = 22$ μm and $I_D = 6.25$ mA, which results in a total VCO core current consumption of 12.5 mA. The bias current is generated using a PMOS current source (MP_1) connected to the central tap of the differential inductor.

The minimum capacitance values of the varactor and switched capacitors, the parasitic parallel capacitance of the inductor and the cross-coupled pair and the capacitances of the output buffer NMOS transistors limit the maximum operation frequency of the VCO. Since the other elements have already been sized, the maximum operation frequency sets a limit to the size of the output buffer transistors. The common source stage is then sized according to this limit. Furthermore, since adding dc blocking capacitors between the VCO core outputs and the buffers would add unacceptable parasitic capacitance, they are

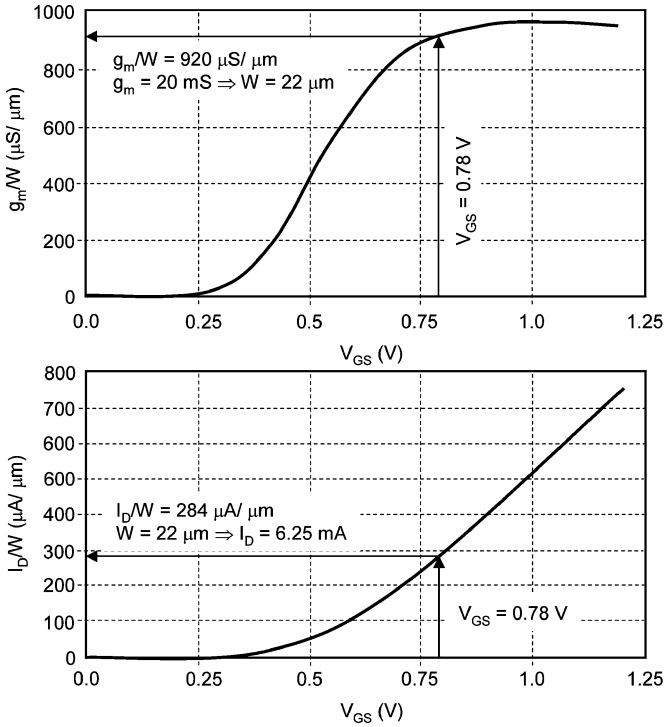


Fig. 3. Minimum length NMOS characteristics. The transistors are low-power low-threshold voltage transistors with gate connected to drain.

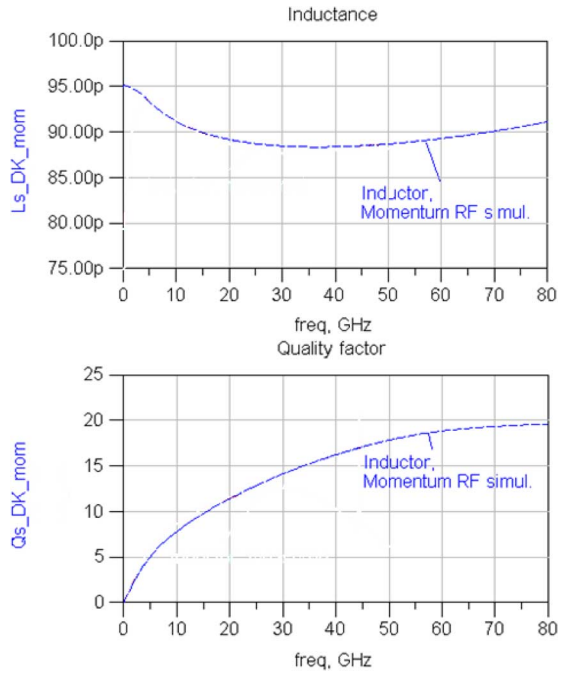


Fig. 4. Inductor momentum RF simulation results.

not dc decoupled and the gate voltage of the common source stage is set by the VCO output voltage. The output buffer is biased by directly connecting at dc the drain of the NMOS transistor to a separate 1.2-V power supply (V_{DD_BUFF}). The connection is open at AC since it is made with a microstrip TL with a length that equals $\lambda/4$ at f_o. The output impedance of the buffer stage is matched to 50 Ω by adjusting the length of the output and ac-shorted stub TLs as described in Section IV.

III. *LC* Tank Components

A. Inductor

The inductor of the tank is a single-turn differential inductor made with the two upper copper metal layers plus the aluminum metallization layer. It has a patterned grounded shield. The inductor was simulated using Agilent Momentum in RF mode (see Fig. 4). The inductance and quality factor at 60 GHz are 90 pH and 18, respectively.

B. Continuous Tuning Varactor

The varactors are implemented using a thick gate–oxide available in the process that provides a capacitance ratio $C_{VF,\max}/C_{VF,\min} \approx 3$ for voltages between 0 and 1.8 V. Fig. 5 shows the simplified varactor cross-section and the capacitance and quality factor curves. It is made with two N+poly/Nwell varactors. The N+poly gates are each connected to one of the two differential terminals (Out+, Out−). They are placed in the same Nwell that is biased using a common voltage (V_c). The differential current path length is thus minimized [14]. Larger values are obtained using an array of $n \times m$ basic cells with a waffle structure for distributing the common signals (V_c and the substrate biasing *Subs*), as shown in Fig. 5.

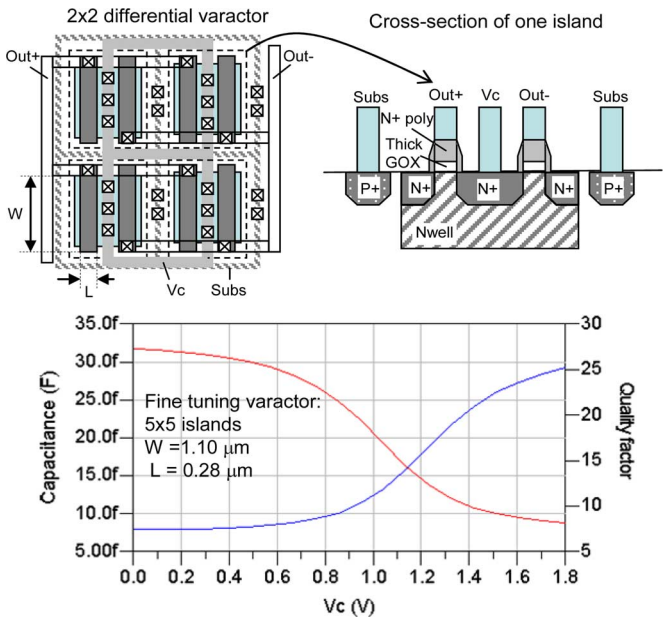


Fig. 5. Fine-tuning differential varactor structure, capacitance [red curve (in online version)] and quality factor [blue curve (in online version)].

C. Discrete Tuning Varactor

The tuning range of the VCO can be extended by adding switched capacitors to the tank. Fig. 6 shows the most usual implementation of the switching control circuitry. The main drawback of this approach is that the NMOS transistors used in the switches contribute significantly to the PN of the oscillator. This paper proposes a novel topology that uses a differential varactor without switches to implement the switched capacitor. The V_c

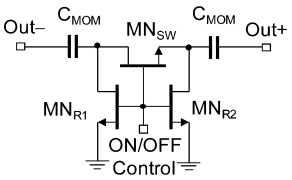


Fig. 6. Conventional differential switched capacitor schematic.

TABLE I
COMPARISON OF SWITCHED MOM CAPACITOR AND SWITCHED VARACTOR

Parameter	Switched MOM capacitors	Switched diff. varactor
Unit cell ON capacitance	2.09 fF	1.98 fF
Unit cell ON quality factor	4.54	4.56
Unit cell OFF capacitance	0.50 fF	0.54 fF
Unit cell OFF quality factor	8.1	16.5
VCO oscillation frequency (4 units ON, 3 units OFF)	60.57 GHz	60.22 GHz
VCO phase noise @1MHz offset	-92.45 dBc/Hz ($9.4\cdot10^{-10}$ V^2/Hz)	-99.46 dBc/Hz ($2.06\cdot10^{-10}$ V^2/Hz)
Contributions to phase noise		
MN_{SW} transistors flicker (ON units)	52% ($4.9\cdot10^{-10}$ V^2/Hz)	-
MN_1 and MN_2 channel noise	11.6% ($1.1\cdot10^{-10}$ V^2/Hz)	43.6% ($0.9\cdot10^{-10}$ V^2/Hz)
MP_1 flicker noise	3.3% ($0.3\cdot10^{-10}$ V^2/Hz)	19.2% ($0.4\cdot10^{-10}$ V^2/Hz)

signal of the varactor is directly connected to a digital signal that switches the varactor ON or OFF by applying 0 or 1.8 V to the gate of the N+poly/Nwell differential varactor. Table I compares the performances of a switched capacitor implemented using both techniques and the contribution to the VCO PN obtained by simulations. In this example, the switched capacitor circuit is implemented using a low-threshold voltage $NM_{\rm SW}$ with a width of 1.5 μm and two standard threshold voltages NM_{R1}, NM_{R2} with a width of 0.6 μm. All transistors have minimum length. The capacitors are 1.63 fF metal–oxide–metal (MOM). The ON and OFF voltage are 1.2 and 0 V, respectively.

The discrete tuning in the VCO is implemented using a binary-scaled set of varactors composed of one, two, and four units controlled by b0, b1, and b3 bits, respectively. The digitally controlled differential varactor unit cell has an ON/OFF capacitance and quality factor of 1.98 fF/0.54 fF and 4.5/16.5, respectively, at 60 GHz. Such a low capacitance is extremely difficult to measure directly. Fig. 7 shows the simulation results obtained using the model provided by the manufacturer, which result in an ON/OFF capacitance change of 1.34 fF for the unit cell. The experimental capacitance change corresponding to one LSB change as indirectly obtained from the oscillation frequency measurements. It varies from 1.26 to 1.07 fF in the lower and higher frequency range of the tuning curves, respectively. This is in acceptable agreement with simulations if one considers that the measurements are done at different frequencies for each digital code. Other voltage-dependent parasitic capacitances that vary with output frequency (because large signal output amplitude varies as well) affect the accuracy of the switched varactor capacitance value derived from the measurements.

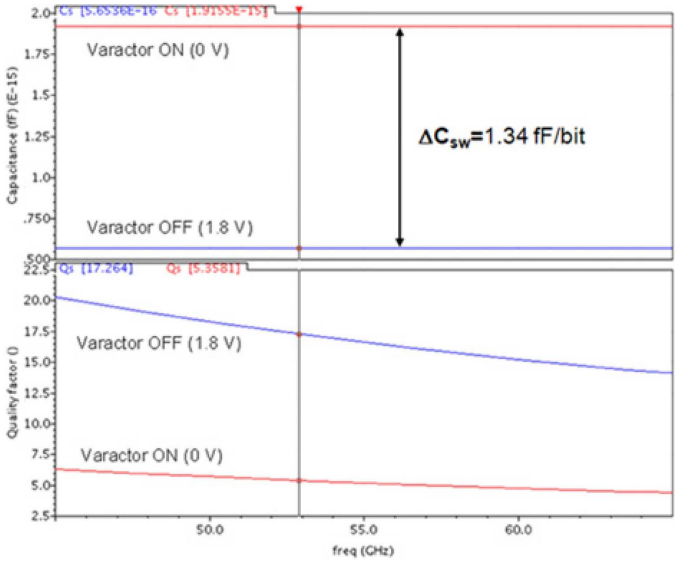


Fig. 7. Simulation of one unit of the digitally controlled differential varactor capacitance and quality factor.

IV. PHYSICAL DESIGN AND MODELING TECHNIQUES

A. Physical Design and Integration of EM Models

The physical design is done simultaneously with the transistor level design and sizing procedure presented in Section II. The layout of the interconnection between the varactors, the inductor, and the active sections of the VCO core and the buffers is optimized to reduce parasitic capacitance and inductance, as shown in Fig. 8. This structure is simulated using an EM simulator (Momentum from Agilent Technologies) to obtain a multiport S-parameter model. The layout is completed with additional recognition layers that associate the physical structure with the model derived from the EM simulation. In this way, the conventional layout-versus-schematic and extraction flows can be used with the full-chip layout. The same modeling technique is used for the inductor, with and without the surrounding structures, and the high-frequency pads. In the case of the inductor, the surrounding structures just increase the inductance at 60 GHz by 1 pH. The netlist resulting from the extraction process contains the S-parameter models for the selected structures, the device models associated with the transistors and varactors pcells, and *RC* parasitic information for the remaining interconnections.

B. Parameterized EM Modeling

The previous approach is suitable for fixed layout structures requiring EM models. However, during the design of the output buffer and the PN filter, the length of the TLs has to be adjusted in the framework of an optimization process run at schematic level. In this case, an alternative modeling approach has been used.

The TL used in this study is illustrated in Fig. 9. This microstrip line is made up of a conducting strip on a dielectric in parallel to a ground plane. In silicon technology, the conducting

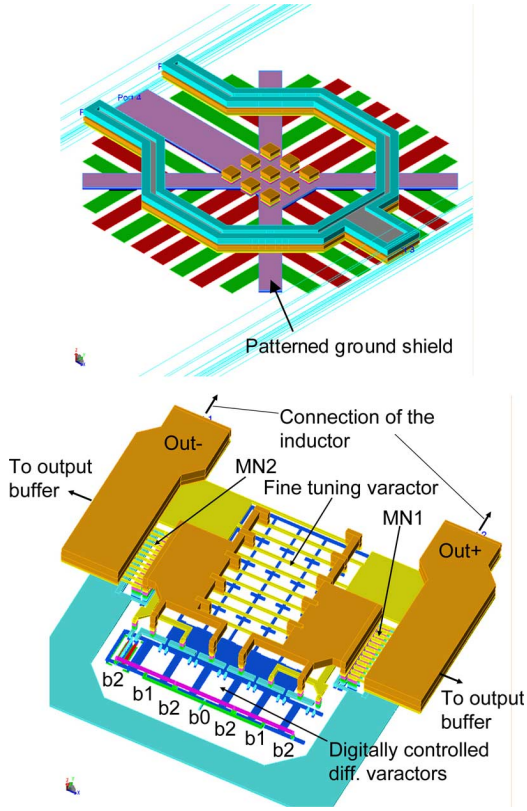


Fig. 8. Inductor layout (*top*) and interconnection of varactors and structure of transistors (*bottom*).

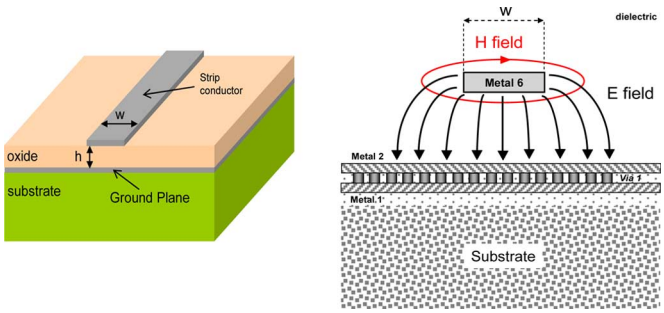


Fig. 9. Illustration of a silicon thin film microstrip line (*left*) and cross section, showing electric and magnetic fields (*right*).

strip is separated from the ground plane by one or several intermetal dielectrics. The electric and magnetic fields are orthogonal in the transverse plane (see Fig. 9).

The microstrip line design is dictated by several requirements. First, the characteristic impedance of a microstrip line depends on its dimensions and the type of dielectric that surrounds it. In the case of 65-nm CMOS technology, the only degrees of freedom for adjusting the characteristic impedance are the width of the line and the choice of the metallization (M1–M6) layers. However, to make microstrip lines in CMOS technology, the choices of width and height are also constrained by the technology design rules. Fig. 9 illustrates the realization of a microstrip line using the top metal level (M6) as a conducting strip and the two bottom metal levels (M1 + M2) as ground plane. In order to fulfill metal density rules, the

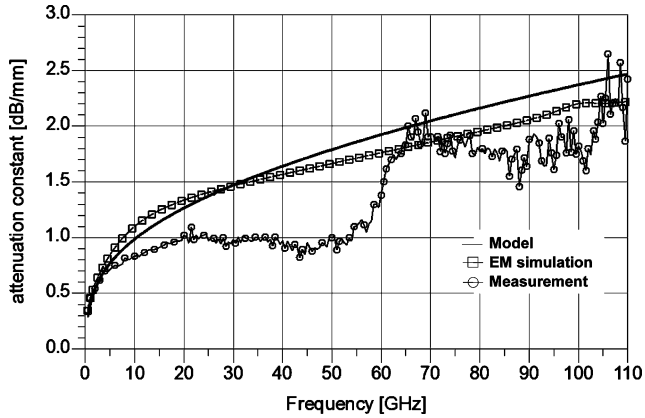


Fig. 10. Comparison of the microstrip line attenuation constant achieved through the measurement, EM simulation, and model used in this paper.

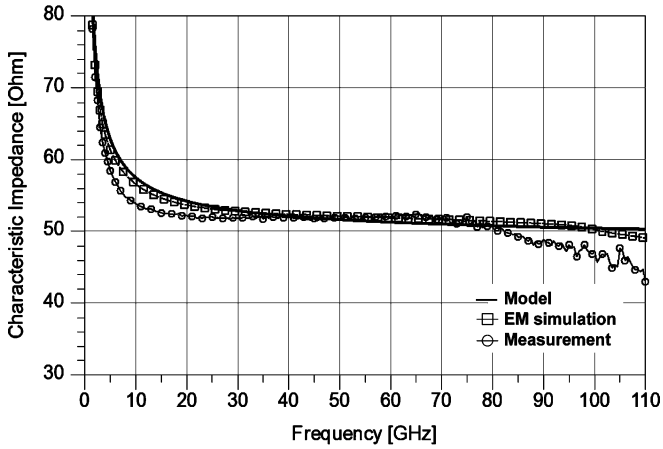


Fig. 11. Microstrip line characteristic impedance comparison between measurement, EM simulation, and model used in this paper.

ground plane is made as a wired mesh. The behavior of this plane is nearly identical to that of a continuous plane since the "holes" opened in the metal layers are smaller than the signal wavelength at these frequencies.

There are no losses due to the substrate on a microstrip line since the ground plane masks it, which prevents the penetration of the EM field in the substrate. In order to reduce the losses, the only remaining degree of freedom is the metallization thickness (if the skin depth is higher than the conductor thickness) and the width of the microstrip conductor. However, taking into account the design rules so as to keep a wide range of characteristic impedances, the only practical option consists of using the last thick metal level (M6) to reduce the series resistance.

Once the microstrip line construction is fixed, the second step consists in using EM simulations to calibrate a parameterized model suitable for sweep analysis and optimization during the schematic design phase. In this paper, the Agilent ADS multilayer model has been used. This model takes into account the microstrip line characteristics described earlier. Figs. 10 and 11 show a comparison between this model, the EM simulations and the measurements. It is clear that this modeling approach offers a very good level of accuracy with a loss difference of less than 1 dB for a TL that is 1 mm in length.

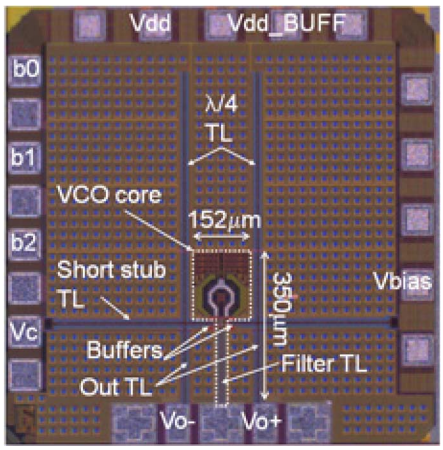


Fig. 12. VCO die micrograph.

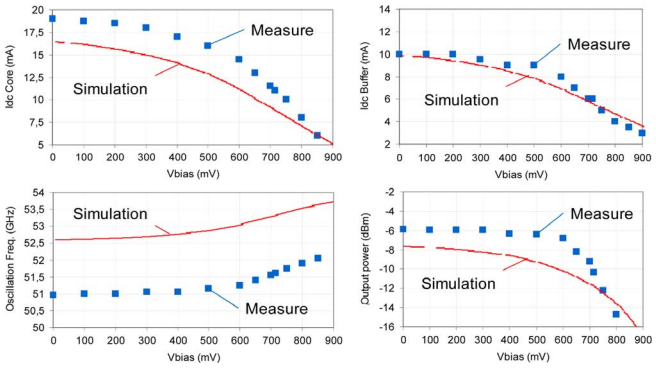


Fig. 13. Simulation and experimental bias analysis of the VCO.

V. Experimental Results

The proposed VCO circuit is implemented in a 65-nm bulk CMOS process. A chip micrograph is shown in Fig. 12. The total chip area is 0.98 mm^2, which is pad limited. The oscillator core fits in a rectangle of 152 μm $\times$ 350 μm, around 0.05 mm^2. The power supply for both the VCO core and output buffers is 1.2 V. They dissipate 15 and 9.6 mW, respectively. The fabricated VCO is measured using wafer contact probes. One of the outputs is terminated with a 50-Ω load and the other one is connected to a 67-GHz spectrum analyzer. The maximum frequency obtained is 60.5 GHz for $V_c = 1.8$ V and digital code "000."Fig. 13 shows a comparison between simulation and measurement data from a bias analysis of the VCO. The voltage that sets the core VCO current is swept from 0 to 0.9 V. There is a good agreement between simulation and experimental results for the bias current and a constant error of 1.5 GHz for the oscillation frequency. This has been quantified as an underestimation of 8.5 fF in parallel with the tank, which represents a 2.5% modeling error. This discrepancy can also be observed in the comparison between the simulated and measured tuning curves, as shown in Fig. 14.

Tuning curves and output power are shown in Fig. 14. Output power (after correcting for the probe and cables losses) is quite

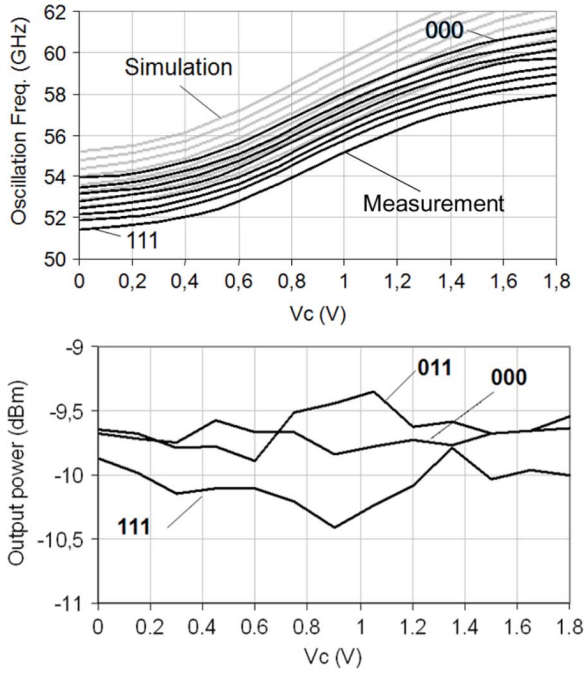
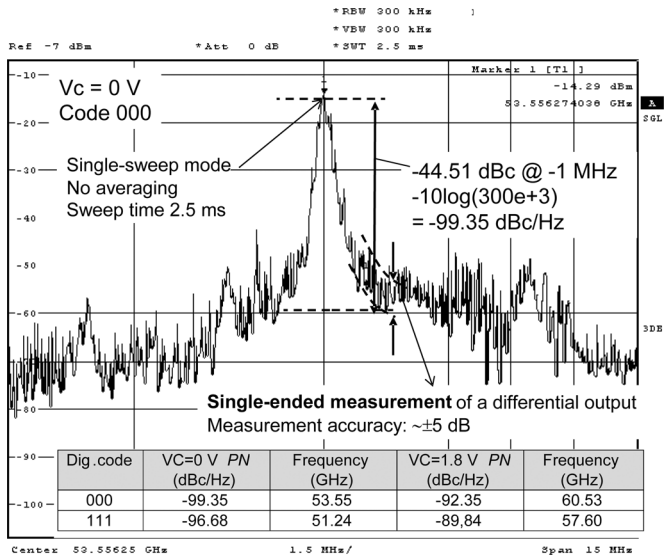


Fig. 14. Measured output frequency and output power versus control voltage and digital code.



Dig.code	VC=0 V *PN* (dBc/Hz)	Frequency (GHz)	VC=1.8 V *PN* (dBc/Hz)	Frequency (GHz)
000	-99.35	53.55	-92.35	60.53
111	-96.68	51.24	-89,84	57.60

Fig. 15. Output spectrum and PN measurements.

constant: -9.8 dBm ± 0.5 dB. Fig. 15 shows the output spectrum corresponding to an oscillation frequency of 53.55 GHz. The PN $\mathcal{L}(\Delta f)$ at a $\Delta f = 1$ MHz frequency offset ranges from -99.35 dBc/Hz for $f_0 = 53.55$ GHz to -89.84 dBc/Hz for $f_0 = 57.60$ GHz, which results in a very competitive FOM of -182.2 dBc/Hz (see Table II). The fine tuning VCO gain varies from 1.5 GHz/V in the extremes to 5.5 GHz/V in the center of the tuning curves. Such a large gain complicates PN measurements, requiring the spectrum analyzer to be operated in single sweep since the VCO is measured in open loop and only single-ended measurement were possible at 60 GHz. Both limitations result in noisy curves, since no averaging or common mode noise cancellation is possible.

TABLE II
COMPARISON WITH PREVIOUS WORKS

Ref	Tech.	Central freq f_o (GHz)	FTR (%)	$\mathcal{L}(\Delta f)$ @ Δf = 1 MHz	P_{DC} (mW)	Oscillator FOM (dBc/Hz)	VCO FOM_T (dBc/Hz)	Technique
[2] ISSCC06	90-nm CMOS	60	0.2	-100	1.9 @ 1 V	-193	-159	Slow-wave mode
[3] JSSC07	0.18-µm CMOS	40	20	-100.2	27 @ 1.5 V	-177.9	-183.9	Standing Wave
[4] JSSC06	0.13-µm CMOS	56.5	9.8	-89	9.8 @ 1.5 V	-174.5	-174.3	MOS varactor
[5] MTT-S04	90-nm SOI	60	14	-94	9.6 @ 1.2 V	-180	-182.7	MOS varactor
[6] ISSCC07	65-nm SOI	70.1	9.55	-106.4 @ 10 MHz	5.4 @ 1.2 V	-175.7	-175.3	MOS varactor
[7] RFIC08	65-nm CMOS	54	11.5	-118 @ 10 MHz	7.2 @ 1.2 V	-184	-185.2	MOS varactor
[8] MTTS 2008	90-nm CMOS	52	6	-95	20 @ 1V	-176	-171	MOS varactor
[9] RFIC08	130-nm CMOS	62	10	-90	3.9 @ 1V	-180	-180	MOS varactor
[10] ICMMT08	130-nm CMOS	67	6	-91	21 @ 1.5 V	-174	-172	MOS varactor
[11] VLSIDAT09	130-nm CMOS	56.5	7	-93 @ 10 MHZ	8 @ 0.8 V	-160	-158	MOS varactor
[12] RFIC 2009	90-nm CMOS	64	8.75	-95	3.2 @ 0.6 V	-186	-185	MOS varactor
This work	**65-nm CMOS**	**56**	**17**	**-99.4**	**15 @ 1.2 V**	**-182.2**	**-186.8**	**MOS varactor**

$$\mathrm{FOM} = \mathcal{L}(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{\mathrm{dc}}}{1\,\mathrm{mW}}\right) \qquad \mathrm{FOM}_T = \mathcal{L}(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{\mathrm{dc}}}{1\,\mathrm{mW}}\right) - 20\log\left(\frac{\mathrm{FTR}}{10\%}\right)$$

VI. CONCLUSION

The fabricated VCO has been forecasted to be used in a 5-GHz low IF (LIF) architecture, and has a central-frequency of 56 GHz. It archives a continuous FTR between 6.53 and 7.15 GHz, depending on the tuning curve selected with the 3-bit digital code. The digital control, which operates directly on the varactor without any additional switch, is able to change the oscillation frequency by an average of 310 MHz/bit when $Vc = 0$ V and 390 MHz/bit when $Vc = 1.8$ V. This corresponds to a capacitance change of 1.07 and 1.23 fF/bit, respectively. Such a small change in capacitance opens the door for digitally controlled oscillators operating at millimeter-wave frequencies since even smaller capacitances can be implemented with this technique [17]. The total tuning range is 9.3 GHz, i.e., 17%, which is larger than any other millimeter-wave *LC*-VCO previously reported [2]–[12]. If the tuning range is taken into account, the VCO results in a state-of-the-art FOM_T of 186.8 dBc/Hz.

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